Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) An image processing system comprising:

a first processing layer ~~adapted~~ operative to perform object-independent processing in real time, wherein said object-independent processing is further ~~adapted~~ operative to include a plurality of processors corresponding to the first processing layer, and wherein each of the plurality of the processors is associated with a different one of pixels of an image frame;

a second processing layer ~~adapted~~ operative to perform object-dependent processing in real time to obtain a dynamic feature set for use in object recognition; and

a third processing layer ~~adapted~~ operative in real time to perform object recognition and association employing said dynamic feature set against an object to be recognized.

2. (Currently amended) The image processing system of claim 1 wherein said object-dependent processing is further ~~adapted~~ operative to be performed by a symmetric multi-processor.

3. (Original) The image processing system of claim 1 wherein the plurality of processors adapted to perform object independent processing form a massively parallel processing system.

4. (Original) The image processing system of claim 3 wherein the massively parallel processing system is a systolic array type massively parallel processing system.

5. (Original) The image processing system of claim 4 wherein the systolic array type massively parallel processing system is configured as a single-instruction multiple-data system.

6. (Currently amended) The image processing system of claim 1 wherein each of the plurality of the processors ~~adapted~~ operative to perform object independent processing is enabled to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

7. (Original) The image processing system of claim 1 further comprising:

an image capturing block.

8. (Original) The image processing system of claim 7 wherein the plurality of processors are formed on a first semiconductor substrate different from a second semiconductor substrate on which the image capturing block is formed.

9. (Currently amended) The image processing system of claim 8 further comprising:

a realignment buffer ~~adapted~~ operative to realign the data received from first and second analog-to-digital converters disposed in the image capturing block.

10. (Currently amended) A method for processing images comprising:

performing object-independent processing in a first processing layer in real time;

performing object-dependent processing in a second processing layer in real time to obtain a dynamic feature set for use in object recognition; and

performing in real time object recognition and association in a third processing layer employing said dynamic feature set against an object to be recognized.

11. (Currently amended) The method of claim ~~10~~ 12 further comprising:

performing object-independent processing by a plurality of processors each associated with a different one of pixels of an image frame being processed.

12. (Currently amended) The method of claim ~~11~~ 10 further comprising:

performing object-dependent processing by a symmetric multi-processor.

13. (Currently amended) The method of claim ~~11~~ 12 further comprising:

performing object independent processing by a plurality of processors that form a massively parallel processing system.

14. (Original) The method of claim 13 wherein the massively parallel processing system is a systolic array type massively parallel processing system.

15. (Original) The method of claim 14 further comprising:

configuring the systolic array massively parallel processing system as a single-instruction multiple-data system.

16. (Original) The method of claim 11 wherein each of the plurality of the processors is enabled to perform a unified and symmetric processing of N dimensions in space and one dimension in time.

17. (Original) The method of claim 11 further comprising:

capturing the image frame on a first semiconductor substrate that is different from a second semiconductor substrate on which the plurality of processors are formed.

18. (Original) The method of claim 17 further comprising

converting analog data corresponding to the image frame to digital data; and

realigning the converted digital data.